LISTING OF THE CLAIMS

Please amend claims 1, 5, 7-8, 11 and 14, and cancel claim 6 as indicated below. This listing of claims replaces all prior versions.

1. (Currently Amended) A semiconductor device including a semiconductor region having p and n semiconductor regions which form a pn junction and a field shaping region located adjacent only one of the p and n semiconductor regions ~~the pn junction~~ to increase the reverse breakdown voltage of the device, wherein the field shaping region is insulating material and ~~is coupled to~~ the field shaping region extends from a first capacitive voltage coupling region ~~and~~ to a second capacitive voltage coupling region[[s]] which are provided to apply, in use, substantially the same voltages as are applied to the pn junction, the material and capacitive coupling of the field shaping region being such that, when a reverse voltage is applied across the pn junction and the device is non-conducting, a capacitive electric field is present in a part of the field shaping region which extends beyond a limit of the pn junction depletion region which would exist in the absence of the field shaping region, the electric field in the field shaping region inducing a stretched electric field limited to a correspondingly stretched pn junction depletion region in the semiconductor region.

2. (Original) A device as claimed in claim 1, wherein the field shaping region insulating material has a dielectric constant greater than that of silicon dioxide.

3. (Original) A device as claimed in claim 2, wherein the field shaping region insulating material has a dielectric constant greater than that of silicon nitride.

4. (Original) A device as claimed in claim 3, wherein the field shaping insulating material is tantalum oxide Ta_2O_5.

5. (Currently Amended) A device as claimed in claim 1, wherein the insulating field shaping region is adjacent ~~only one of the p side and~~ the n semiconductor region ~~side of the pn junction~~.

6. (Cancelled) A device as claimed in claim 1, wherein the insulating field shaping region is adjacent and bridges both the p side and the n side of the pn junction.

7. (Currently Amended) A device as claimed in claim [[5]] 1, wherein ~~there is a~~ said insulating field shaping region is adjacent only one side of the n semiconductor region ~~lateral extent of the pn junction~~.

8. (Currently Amended) A device as claimed in claim [[5]] 1, wherein ~~there is a~~ said insulating field shaping region is adjacent both sides of the n semiconductor region ~~lateral extent of the pn junction~~.

9. (Previously presented) A device as claimed in claim 1, wherein at least one of the first and second capacitive voltage coupling regions comprises one of the p and n semiconductor regions which form the pn junction.

10. (Previously presented) A device as claimed in claim 1, wherein at least one of the first and second capacitive voltage coupling regions comprises a more highly doped semiconductor region of the same conductivity type and adjacent one of the p and n semiconductor regions which form the pn junction.

11. (Currently Amended) A device as claimed in claim 1, wherein at least one of the first and second capacitive voltage coupling regions comprises a conductive material region.

12. (Previously presented) A device as claimed in claim 11, wherein the conductive material region is integral with a main electrode of the device.

13. (Previously presented) A device as claimed in claim 1, wherein the capacitively coupled insulating field shaping region is separated by an insulating region from the semiconductor region having the pn junction.

14. (Currently Amended) A device as claimed in claim 1, wherein the device is a diode device and the pn junction is the rectifying junction of the diode device.

15. (Previously presented) A device as claimed in claim 1, wherein the device is a bipolar transistor and the pn junction is the junction between the base region and a collector drift region of the device.

16. (Previously presented) A device as claimed in claim 1, wherein the device is a field effect transistor and the pn junction is the junction between the channel accommodating body region and a drain drift region of the device.

17. (Previously presented) A device as claimed in claim 15, wherein the drift region is non-uniformly doped.

18. (Previously presented) A device as claimed in claim 15, wherein the stretched pn junction depletion region extends only partly through said drift region.